**Job Description 1**

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| **ASIC Tools/Methods Application Engineer** **-** **770107  (Seoul)**  **Description**  The ASIC Tools/Methods Application Engineer (AE) will provide high quality design automation solutions and technical support to Intel Custom Foundry (ICF) customers in the ASIC design area. The candidate will work with foundry customer design team to design, develop and support the most competitive computer-aided design (CAD) solutions and methodology for customers' design in Intel-based technology. The candidate will be responsible for driving methodology, innovations and productivity improvements in design flows while working with vendors on feature development and bug resolution. Specific ASIC Tools/Methods AE responsibilities include:   * Drive the development of and/or co-develop tools and methodology that enable our foundry customers to realize their full potential with Intel 22nm, 14nm and/or 10nm process technology. * Provide high quality technical support to ICF customers covering areas such as Logic Synthesis, Placement, Routing and Timing. * Quickly ramp our first-time customers and external eco-system partners on the design flow, techniques and recipes for implementing high quality and proficient designs on Intel technology. * Work with global ICF development teams to develop the ASIC design capabilities and solutions needed to deliver the most competitive solutions for our foundry customers.   **Qualifications**   * Bachelor, Master or Doctorate degree in relevant fields with 5 to 10 years of experience in hands-on role in netlist-to-GDS activities of complex ASIC development projects. * Strong programming and scripting knowledge and experience with PERL, TCL and shell scripting. * Strong ability to develop design recipe, scripts, macros and solutions for ASIC design. * A wide breadth of ASIC design knowledge is required and experience with external ASIC design tools and solutions is a plus * In depth understanding of product development on leading edge process technologies with a strong preference for hands on experience with Intel process technologies * Excellent communication skills for communicating and delivering training on design/process requirements to customers/vendors * Proven track record of uncompromising customer orientation to deliver leading-edge solutions * Ability to work effectively with matrix global teams in a variety of geographies   If you are keen, please email your resume to faith.gan@intel.com or apply directly at <https://intel.taleo.net/careersection/10000/jobdetail.ftl?job=770107> |

**Job Description 2**

**ASIC Design Application and Solution Engineer** **-** **770098** **(Seoul)**

**Description**

The ASIC Design Application and Solution Engineer (ASE) is the primary interface for Intel Custom Foundry (ICF) customers in the area of ASIC design. The candidate will provide high quality ASIC design solutions, services and technical support to ICF customers and enable our foundry customers to realize their full potential with Intel 22nm, 14nm and/or 10nm process technology. Specific ASIC Design ASE responsibilities include:

* Provide high quality ASIC design solutions, services and technical support to ICF customers covering areas such as Logic Synthesis, Placement, Routing and Timing.
* Quickly ramp our first-time customers and external eco-system partners on the design flow, techniques and recipes for implementing high quality and proficient designs on Intel technology.
* Provide in-depth technical advice and hands-on guidance to design engineers from customer's team as well as performing design study and execution on customers' complex and critical design blocks.
* Channel customer design issues and constraints to internal development teams and co-define the ASIC design capabilities and solutions needed to deliver the most competitive solutions for our foundry customers.
* Improve overall quality of service to our foundry customers through enhanced technical documentation and efficient customer issue resolution processes.

**Qualifications**

* Bachelor, Master or Doctorate degree in relevant fields with 5 to 10 years of experience in hands-on role in netlist-to-GDS activities of complex ASIC development projects
* In-depth understanding of ASIC design methodologies, design flows, and design collateral is a required skill.
* Expert level hands-on experience with Logic Synthesis, Automated Place-and-Route, Physical Verification (LVS/DRC), Static Timing Analysis (STA) and Full-Chip Integration
* Proven track record of uncompromising customer orientation to deliver leading-edge solutions
* In depth understanding of product design and development on leading edge silicon technologies
* In depth understanding of the external Foundry and eco-system design enablement offerings and trends is a significant plus   
  Complex problem solving and decision making with a proven record of results orientation
* Ability to work effectively with global teams in a variety of geographies
* Excellent communication skills with an ability to synthesize complex info into easy to digest form for senior executives

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**Job Description 3**

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| **Analog Layout Design Engineer** **–** **770108 (Seoul)**  **Description**  The key function of this position will be physical design with strong focus on analog layout design using industry standard EDA tools. The candidate will be in a key position interacting with ICF customers to understand and scope their needs and provide excellent, timely technical support and consultation.  The candidate will   * Engage in the layout design work for customer and improve the layout quality of customers' design. * Need excellent communication skills to provide training, advice and guidance to mask designers on layout design in Intel process nodes. * Be a key part of the function will be to collect best known methods, write training materials and conduct training to mask designers and also walk through layout design of critical layout work in collaboration with design teams. * Contribute to productivity improvements for efficient layout design by providing feedback to tools and methodology developers.   **Qualifications**   * Engineering degree in Electrical/Electronics/Computers. However, key experience in industry standard layout tools and methodology can be a good substitute. * Minimum of 5 to 10 years of analog layout design with strong background in layout design and planning for advanced technology nodes is required. * Working experience in analog circuit/layout design and experience leading other mask designers. * Experience taking a design through verification on advanced technology nodes. Experience ranging from leaf level cell design to integration is desired. * Foundation in best layout practices for analog circuit layouts design. * Excellent communication skills in order to communicate and deliver training on Intel process requirements to customers/vendors. |

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**Job Description 4**

**Memory Design Application and Solution Engineer** **–** **770110 (Seoul)**

**Description**

 The candidate will be the primary interface and first line support to external Intel Foundry (ICF) customers and vendors in the memory design area. The candidate will work with foundry customer design team to design, develop and support memory design using Intel technology. The responsibilities of this position include:

* Deliver high quality solutions, services and support to our external foundry customers and vendors on the memory design and design capabilities
* Quickly ramp our first time customers and external eco-system partners to enable high quality and proficient design on Intel-based technology
* Work with global development teams to define the design capabilities and solutions needed to deliver the most competitive solutions for our foundry customers.
* Improve overall quality of service to our foundry customers through enhanced technical documentation and efficient customer issue resolution processes.

**Qualifications**

* Bachelor, Master or Doctorate degree in relevant fields with 5+ years of experience in hands-on role in memory design.
* In depth understanding of product development on leading edge process technologies with a strong preference for hands on experience with Intel process technologies
* Excellent communication skills for communicating and delivering training on design/process requirements to customers/vendors
* Proven track record of uncompromising customer orientation to deliver leading-edge solutions
* Ability to work effectively with matrix global teams in a variety of geographies

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**Job Description 5**

**Extraction/Runsets/Fill Application Engineer** **–** **77019 (Seoul)**

**Description**

The candidate will be the primary interface and first line support to external Intel Foundry (ICF) customers and vendors in the areas of extraction, runsets and fill. The candidate will work with foundry customer design team to design, develop and support the most competitive computer-aided design (CAD) solutions and methodology for customers' design in Intel-based technology in the extraction, runsets and fill areas. The candidate will be responsible for driving methodology, innovations and productivity improvements in design flows while working with vendors on feature development and bug resolution. Specific responsibilities include:

* Drive the development of and/or co-develop tools and methodology that enable our foundry customers to realize their full potential with Intel 22nm, 14nm and/or 10nm process technology.
* Provide high quality technical support to ICF customers covering the extraction, runsets and fill areas
* Quickly ramp our first-time customers and external eco-system partners on the extraction, runsets and fill design toots/flows for high quality and proficient designs on Intel technology.
* Work with global ICF development teams to develop the extraction, runsets and fill design capabilities and solutions needed to deliver the most competitive solutions for our foundry customers.
* Improve overall quality of service to our foundry customers through enhanced technical documentation and efficient customer issue resolution processes.

**Qualifications**

* Bachelor, Master or Doctorate degree in relevant fields with 5+ years of experience in hands-on role in the extraction, runsets and fill areas.
* Strong programming and scripting knowledge and experience with PERL, TCL and shell scripting.
* In depth understanding of product development on leading edge process technologies with a strong preference for hands on experience with Intel process technologies
* Excellent communication skills for communicating and delivering training on design/process requirements to customers/vendors
* Proven track record of uncompromising customer orientation to deliver leading-edge solutions
* Ability to work effectively with matrix global teams in a variety of geographies

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