2023

School of EE Lab Introductions

Circuit

KAIST EE

⟨Professor Kyeongha Kwon⟩

THE
KWON GROUP

■ **Contact information**

Professor	**Email: kyeongha@kaist.ac.kr**	**Tel: 7467**
Lab.	**Nanofab Center, 204**	**Tel: 7567/7667**
Website	**https://krg.kaist.ac.kr**	

■ **Current state of the Lab. (in 2023 Spring Semester)**

PhD Student: 2 Master's Student: 9

■ **Research Areas**

▷ **Battery Management System (BMS)**

- Maximize the remaining useful life (RUL) for entire multi-storage platform
- Development of cell state prediction techniques with high stability
- Ongoing research topics:
  - ✓ EV/ESS battery management IC: Measurement & Power Control
  - ✓ Advanced diganosis device (e.g. EIS system) for safety
  - ✓ Algorithm optimization for embbeded system

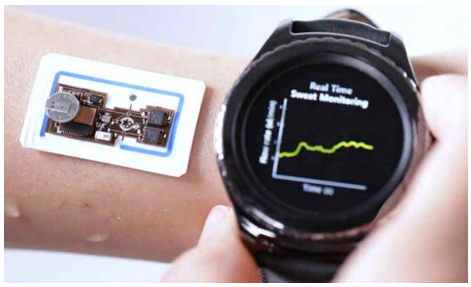
▷ **Medical Application Specific Integrated Circuits (M-ASIC)**

- Real-time monitoring of physical condition using small, wireless and low-power devices
- Flexible, skin-attachable systems to sense various biosignals
- Ongoing research topics:
  - ✓ Blood flow rate monitoring
  - ✓ Capnography: sensing CO2 concentration
  - ✓ Wireless power transfer for implanted cardiac stents

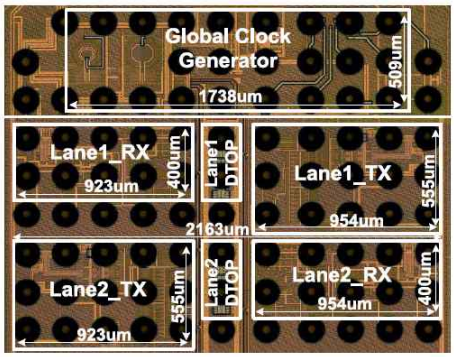
▷ **High-Speed Transceivers**

- Signal distortion due to channel and other environmental causes, resulting erroneous data at receiver
- Distortion compensation in transceiver ICs
- Ongoing research topics:
  - ✓ Crosstalk cancellation for PIM (Processing-in-Memory)
  - ✓ Dispersion compensation for optical communication
  - ✓ Low power on-chip transcievers

<Battery management system on EV>



<Sweat flow monitoring device>



<High speed transceiver die photo>

■ **Recommended courses & Career after graduation**

- Courses on circuits, signals and communcations: EE201, EE304, EE372, EE403, EE202, EE303, EE321, etc. (More information on our website)
- Potential career options after graduation include government-funded/private research institutes or companies related to IC design, medical devices, automobile, etc.

■ **Introduction to the Lab.**

- Horizontal organizational structure and lively workplace atmosphere.
- Lab members with friendly relationship
- Group lunch/dinner and birthday celebrations
- Regular participation in workshops and seminars

■ **Recent research achievements (2023)**

"ASIL-D compliant Battery Monitoring IC with High Measurement Accuracy and Robust Communication," ***IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers***, 2023.

"Battery-free, cardiovascular implant for wireless monitoring of arterial/ventricular pressure, flow rate and temperature in real-time fashion," ***Nature Biomedical Engineering*** (IF:29.234), April 2023.

"Bioresorbable, wireless, and battery-free system for electrotherapy and impedance sensing at wound sites," ***Science Advances*** (IF:14.957), vol. 9, no. 8, Feb. 2023.

<Professor Lee-Sup Kim's Lab.>

Multimedia VLSI Laboratory

■ Contact information

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LAb.	**Email:** cockatiel@kaist.ac.kr	**Tel:** 042-350-5460
Website	http://mvlsi.kaist.ac.kr	

■ Current state of the Lab. (in 2023 Fall Semester)

Postdoctoral Fellows : 0 PhD Students: 3 Master's Student: 5

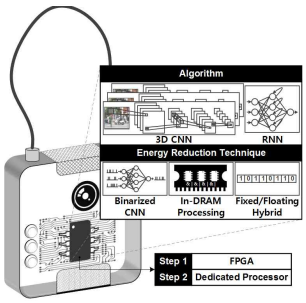
■ Research Areas

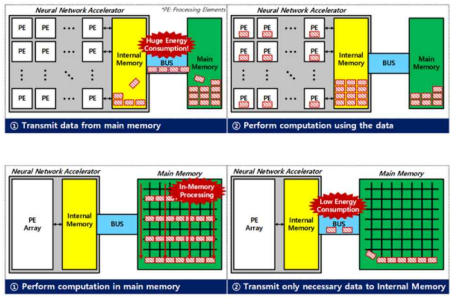
[Deep Learning & Neural Network Processor Design]

Deep learning algorithm is getting a huge attention recently. GPUs are widely used to run neural networks, but it is not appropriate to be integrated in mobile devices like smartphones, wearable devices, and drones because of its low energy-efficiency. We focuses on the design and implementation of a dedicated neural network processor in a both high-performance and energy-efficient way. To this end, researches on the datapath and memory architecture optimized for neural network, a flexible hardware architecture to handle a wide variety of neural network models, and hardware-friendly neural network algorithm are being performed. Finally, a neural network processor chip based on our ideas is designed, fabricated, and tested. We are performing state-of-the-art researches at the most recognized conference.

[Processing in-Memory for Deep Learning]

The conventional Von-Neumann architecture severely suffers from memory bottleneck issue in processing memory-dominant deep learning algorithms since massive amount of data should be transferred through the narrow bus from the main memory to the processor. Meanwhile, processing in-memory (PIM) technique which obeys Non-Von Neumann architecture processes data in the memory and transfers only necessary data to the processor, reducing the energy cost of memory transfers. Therefore, processing in-memory paradigm is the key direction and the next generation platform for efficient processing of large-scale deep neural networks.





■ Recommended courses & Career after graduation

▷ Recommended courses: Digital System, Computer Architecture, Digital Integrated Circuit, Computer Vision, Courses related to Deep Learning & Neural Network

▷ Career: Semiconductor Industries and Institutes (Samsung, SK hynix, Qualcomm, NVIDIA, ETRI, etc.)

■ Introduction to other activities besides research

▷ Coffee break after lunch
▷ Various hobbies with members
▷ Annual summer/winter field trips

■ Introduction to the Lab.

We perform a wide range of researches that covers whole SoC design parts including digital processors, memory architectures. This is our own unique strength that you never see in other laboratories. Therefore, we have a great research environment to bring yourself to a brilliant processor engineer with a capability to design a whole processor system. Our members are encouraged to perform their own researches with freedom in a family-like atmosphere. As a result, we produce the state-of-the-art research performances with international conference and journal papers.

■ Recent research achievements (2023)

[1] The most recognized journal: Myeonggu Kang, Hyein Shin, Junkyum Kim, Lee-Sup Kim, "MGen: A Framework for Energy-Efficient In-ReRAM Acceleration of Multi-Task BERT", *IEEE Transactions on Computers,* accepted, 2023

[2] The most recognized conference: Junkyum Kim, Myeonggu Kang, Yunki Han, Yanggon Kim, Lee-Sup Kim "OptimStore: In-Storage Optimization of Large Scale DNNs with On-Die Processing", *IEEE International Symposium on High-Performance Computer Architecture,* Feb 2023

<Professor Joo-Young Kim's Lab.>

CastLab

■ Contact information

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Lab. : E3-2 #4209 TEL : N/A

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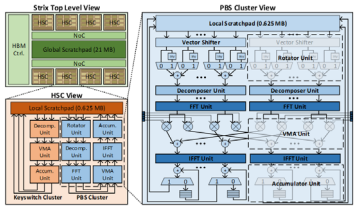
■ Current state of the Lab. (in 2023 Fall Semester)

Postdoctoral Fellows : 0 PhD Students: 14 Master's Student: 16

■ Research Areas

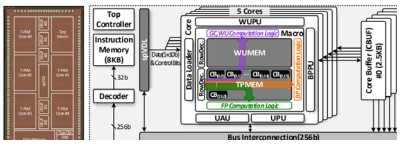
1. Neural Processing Unit

Neural Processing Unit (NPU) is AI-specialized hardware vital for edge and cloud computing. As AI usage grows, dedicated hardware becomes crucial for faster computations. In the cloud, Fully Homomorphic Encryption (FHE) enhances data privacy through encrypted computation, complementing AIaaS. However, current hardware acceleration is insufficient for FHE due to complexity, necessitating specialized architecture. Similarly, in edge scenarios like robotics, reinforcement learning demands real-time, energy-efficient processing, highlighting the need for dedicated hardware solutions.



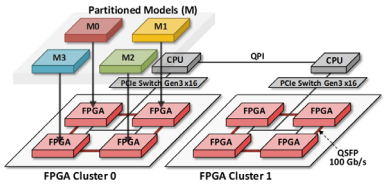
2. Processing in Memory

Traditionally, CPUs performed arithmetic and logic calculations, while memory stored data. However, technology scaling now results in compute units outpacing memory in speed, making data movement the bottleneck. The memory-centric approach, such as Processing – in - Memory (PIM), integrates computation into memory to avoid data movement, visible across hardware levels like main memory and cache using DRAM and SRAM devices. This trend aims to alleviate the data movement problem and enhance system efficiency.



3. Server Appliance

Cloud computing is reshaping enterprise operations with virtualized internet-based infrastructure. Data centers play a pivotal role in this, hosting myriad servers and storage. The surge in AI services necessitates high-efficiency systems, driving data centers toward multi-FPGA appliances for acceleration. In multi-FPGA research, the goal is a flexible server infrastructure that speeds up data center services and enables customized system design, offering re-programmable hardware for evolving operations at lower redesign and cost compared to ASIC or GPU-based solutions.



■ Recommended courses & Career after graduation

- **Recommended Courses:** Digital System Design (EE303), Computer Architecture (EE312), Digital Electronic Circuits (EE372), Courses related to deep learning algorithms.
- **Career:** Silicon companies (Samsung, Apple, IBM) and IT companies (Microsoft, Google, Meta).

■ Introduction to other activities besides research

Beyond research, we enjoy a lot of activities including gatherings like strawberry parties, lunch buddies, and hiking; celebratory events for graduations and birthdays; sports like football and basketball.

■ Introduction to the Lab.

We aim to innovate modern computing systems through hardware specialization. To this end, we are focusing on co-design of multiple layers of computing system such as application, architecture, circuit, and technology.

■ Recent research achievements ('21~'23)

"Strix: An End-to-End Streaming Architecture with Two-Level Ciphertext Batching for Fully Homomorphic Encryption with Programmable Bootstrapping," IEEE/ACM Symposium on Microarchitecture (MICRO), 2023.

"PRIMO: A Full-Stack Processing-in-DRAM Emulation Framework for Machine Learning Workloads," IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2023.

"South Korea's Nationwide Effort for AI Semiconductor Industry," Communications of the ACM (CACM), 2023.

"SP-PIM: A 22.41TFLOPS/W, 8.81Epochs/Sec Super-Pipelined Processing-In-Memory Accelerator with Local Error Prediction for On-Device Learning," Symposium on VLSI Technology and Circuits (VLSI), 2023.

"LightTrader: A Standalone High-Frequency Trading System with Deep Learning Inference Accelerators and Proactive Scheduler," IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2023.

"DFX: A Low-latency Multi-FPGA Appliance for Accelerating Transformer-based Text Generation," IEEE/ACM Symposium on Microarchitecture (MICRO), 2022.

"T-PIM: An Energy-Efficient Processing-In-Memory Accelerator for End-to-End On-Device Training," IEEE Journal of Solid-State Circuits (JSSC), 2022.

"A Dual-Mode Similarity Search Accelerator based on Embedding Compression for Online Cross-Modal Image-Text Retrieval," IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2022.

<Professor Hyun-Sik Kim's Lab.>

Circuit Lab

Electrical Engineering | KAIST

■ **Contact information**

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■ **Current state of the Lab. (in 2023 Fall Semester)**

Ph.D. Students : 13 Master/Ph.D.-Integrated Students: 1 Master's Student: 7

■ **Research Areas**

Our research group is focused on innovations in the CMOS integrated chip designs of analog IC, DDI, PMIC, ROIC, and CIS. And, ultimately we plan to build a complete system-on-a-chip solution by incorporating our knowledge in those fields.

☐ **Power Conversion and Management IC (PMIC)**

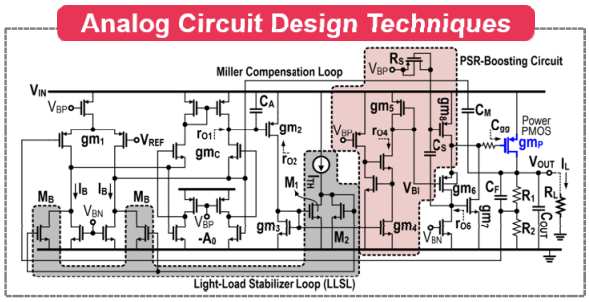
- Switch-mode DC-DC power converter using inductive, capacitive, and hybrid techniques
- Fully-monolithic high-speed switching PMIC for modern SoCs
- Energy-harvesting interface circuit and system
- Fast-response high-PSR low-dropout (LDO) regulator
- Battery charger and management circuit

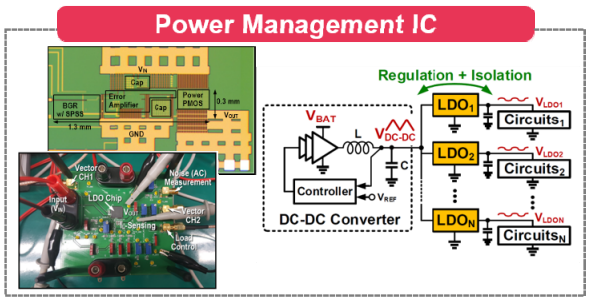
☐ **Display Driving Circuits and Systems**

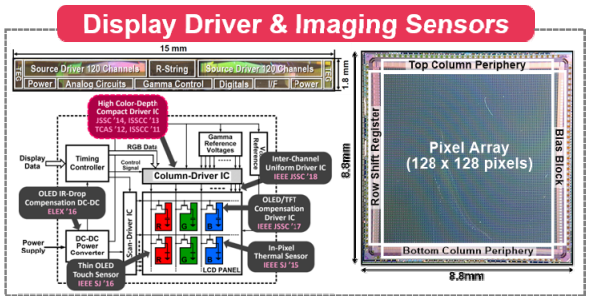
- High-resolution area-efficient digital-to-analog converter (DAC)
- OLED display driver with pixel-readout and active-compensation
- Low-power high-speed output driving buffer amplifier
- Fully-integrated system-on-wafer (SoW) for micro-LED displays
- Displays with touch-sensing functionality

☐ **Readout IC (ROIC) and Imaging Sensor**

- Low-noise high-sensitivity readout circuit and system
- Ultra-high-speed time-delayed integration (TDI) image sensor
- Photon-counting detector for nuclear particles and X-ray







■ **Recommended courses :** Circuit Theory, Electronic Circuits, Analog Electronic Circuits, Analog Integrated Circuits, Power Electronics, Digital Circuits

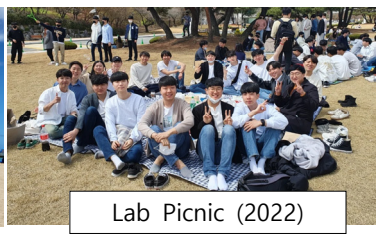
■ **Careers after graduation :** Samsung, LG, SK-Hynix, Research Institute, Silicon-Valley, Academia, University

■ **Introduction to our laboratory**

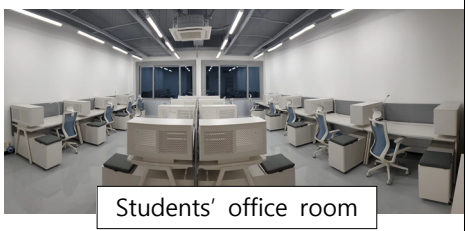
Young and active research environments, Horizontal peer relationship, 24-hours academic discussion, Opened and wide opportunities to attend international conference, Summer/Winter workshop, Refreshed clean office room

■ **Lab. Photo**

VLSI 2022 (Hawaii)



Lab Picnic (2022)



Students' office room

■ **Recent research achievements (2020~2023)**

- Conference Presentations: (top) ISSCC 7편, (top-tier) VLSI Symposium 11편, (major) CICC 1편, (major) ESSCIRC 1편
- Journal Publication: IEEE JSSC 9편, IEEE TPEL 1편, IEEE SSC-L 5편, IEEE SSC-M 1편
- Awards: 반도체설계대전 국무총리상, 삼성휴먼테크 은상(21) & 동상(22), 삼성디스플레이논문대회 금상(22) & 금상(21)

<Professor Seung-Tak Ryu's Lab..>

MSICL
Mixed Signal IC Laboratory

Mixed Signal Integrated Circuits Laboratory

■ **Contact information**

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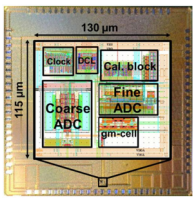
Lab. : E3-2 #4230, 4224 TEL : 042-350-7525, 7625
Website : http://msicl.kaist.ac.kr

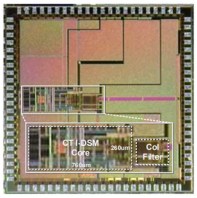
■ **Current state of the Lab. (in 2023 Fall Semester)**

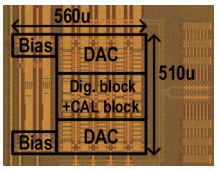
Postdoctoral Fellows : 0 PhD Students: 14 Master's Student: 7

■ **Research Areas**



<10b 500MS/s Pipelined SAR ADC>


<400kS/s 4-ODE CT I-DSM ADC>



<12b 1GS/s CS-DAC w/ cal.>

MSICL researches Analog/Mixed signal circuit design. The major research topic is data converters, which converts analog signal to digital signal or vice-versa. This research area has gained significance along with semiconductor advancements. As digital circuits gain popularity for their enhanced computational capabilities and reduced power consumption, analog circuits assume a pivotal role in transferring natural signals to digital systems. Since numerous signals in human-related contexts remain analog, the research on analog circuits is essential with the development of circuit systems. However, the number of analog circuit designer is insufficient compared to analog circuit demands.

The research scope of MSICL encompasses a range of subjects including: High-speed ADCs (SAR/Pipeline/Flash/Time-domain/Time-Interleaved/etc.) and DACs (Current-domain), High-resolution ADCs (Delta-Sigma Modulator/Noise-shaping SAR), Radiation-tolerant Data converters, Synthesizable Data converters, Design Automation, Random Number Generator, and more.

■ **Recommended courses & Career after graduation**

Since the research of MSICL deals with both analog and digital circuits, the recommended courses are Electronic Circuits (EE304), Digital Electronic Circuits (EE372), and Analog Electronic Circuits (EE403).

■ **Introduction to other activities besides research**

To foster the friendship of lab members, numerous events are organized throughout each season. During spring and fall, outings are arranged, while in summer and winter, regular workshops take place.

■ **Introduction to the Lab.**

As aforementioned, MSICL researches Analog/Mixed signal circuit designs. Data converters which is the major topic of our Lab becomes more important in IC system and undergoes lack of manpower. Since our circuit design treats both analog and digital circuits, the students who have interests in circuit design can get a good chance to study IC circuits. Also, MSICL performs the many projects with companies and researching institute such as Samsung, Hynix, ETRI and so on. So the students can improve the executive ability as well.

■ **Recent research achievements ('21~'23)**

[1] Kent Edrian Lozada*, Dong-Hun Lee*, "A 25kHz-BW 97.4dB-SNDR 100.2dB-DR 3rd-order SAR-Assisted CT DSM with 1-0 MASH and DNC," IEEE ASSCC, 2023.
[2] Jae-Hyun Chung, "An 81.2dB-SNDR Dual-Residue Pipeline ADC with a 2nd-Order Noise-Shaping Interpolating SAR ADC," IEEE CICC, 2023.
[3] Chang-Un Park, "A 12-bit 1GS/s Current-Steering DAC with Paired Current Source Switching Background Mismatch Calibration," IEEE CICC, 2023.
[4] Kent Edrian Lozada, "A 4th-Order Continuous-Time Delta-Sigma Modulator with Hybrid Noise-Coupling," IEEE TCAS-II, 2022.
[5] Kent Edrian Lozada, "A 4th-Order Continuous-Time Delta-Sigma Modulator with Hybrid Noise-Coupling," IEEE MWSCAS, 2022.
[6] Dong-Jin Chang, "A Relative-Prime Rotation Based Fully On-Chip Background Skew Calibration for Time-Interleaved ADCs," IEEE VLSI-C, 2022.
[7] Dong-Ryeol Oh, "A 7-bit Two-Step Flash ADC With Sample-and-Hold Sharing Technique," IEEE, JSSC, 2022.
[8] Dong-Jin Chang, "MixedNet: Network Design Strategies For Cost-Effective Quantized CNNs," IEEE, Access, 2021.
[9] Ye-Dam Kim, "A 4th-Order CT I-DSM with Digital Noise Coupling and Input Pre-Conversion Method for Initialization," IEEE ASSCC, 2021.
[10] Seungyong Lim, "An Input-Buffer Embedding Dual-Residue Pipelined-SAR ADC with Nonbinary Capacitive Interpolation," IEEE ASSCC, 2021.
[11] Dong-Jin Chang, "A 28-nm 10-b 2.2-GS/s 18.2-mW Relative-Prime Time-Interleaved Sub-ranging SAR ADC with On-Chip Background Skew Calibration," IEEE, JSSC, 2021.

⟨Professor In-Cheol Park's Lab⟩

Integrated Computer Systems Laboratory

■ Contact information

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Website	**http://ics.kaist.ac.kr/**	

■ Current state of the Lab. (in 2023 Fall Semester)

Postdoctoral Fellows : 0 PhD Students: 1 Master's Student: 5

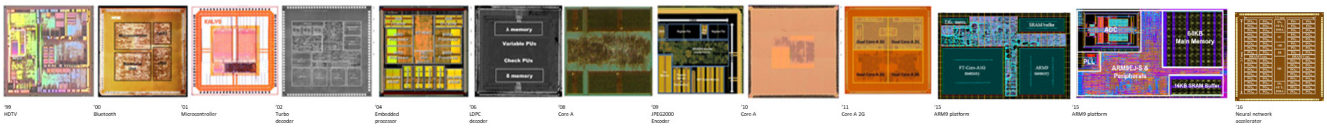
■ Research Areas

Intelligence Computing Systems Laboratory (ICSL) was established in 2000 by Professor In-Cheol Park. The research focus of ICSL is on computer architecture, embedded processors, and VLSI architectures for computationally intensive function blocks, such as multimedia signal processing and communication system. The current research scope of ICSL is VLSI designs for error correcting code blocks, deep neural networks, and communication systems.

• Design of microprocessors: Many kinds of processors were developed such as single-chip programmable SoC platform, and multithread embedded processor. A SoC platform based on 32-bit embedded processor and on-chip bus was developed together with its corresponding development environment including software.

• VLSI design for error-correcting codes: Error correction is one of the most important techniques used in communication and storage systems to recover messages corrupted in noisy environments. In addition, low-power LDPC decoders optimized for NAND flash were devised. Also, LDPC and polor decoders for communication standards such as 5G-NR were developed to achieve near-optimal error-correcting performance with high throughput.

• VLSI design for neural networks: The neural network accelerators were proposed to achieve high energy efficiency while supporting the scalable structure, which can compute a neural network algorithm in multiple processors. In addition, processing-in-memory hardware architecture was designed to achieve high energy efficiency.



■ Recommended courses & Career after graduation

'Digital system design', 'Digital signal processing', 'Signals and systems', 'Introduction to computer architecture', and 'Electronic circuits' are recommended as prerequisite courses. Most graduates are employed as professors or as researchers in major companies such as Samsung Electronics, SK Hynix, Google, Meta (Facebook), and Apple or national research centers such as ETRI and ADD.

■ Introduction to other activities besides research

Our laboratory members enjoy out-of-study activities. We usually go out for dinner. We sometimes go out for drinks.

■ Introduction to the Lab.

ICSL provides one personal PC (Intel Core i7, 32GB RAM), two FULL HD monitors, 512GB SSD, and 1TB HDD per person, and servers for simulations and EDA tools. We have one project and one research meetings every week, which provide proper guidance for works and researches. Our research topics focus on everything related to VLSI architectures including communications systems, storage systems, neural networks and error-correction codes.

■ Recent research achievements (2021-2023)

[1] Suchang Kim et al, "A CNN Inference Accelerator on FPGA With Compression and Layer-Chaining Techniques for Style Transfer Applications", IEEE Transactions on Circuits and Systems-I: Regular Papers, vol. 70, no. 4, pp. 1591-1604-982, Jan. 2023.

[2] Seongjin Lee et al, "Multi-Mode QC-LDPC Decoding Architecture With Novel Memory Access Scheduling for 5G New-Radio Standard", IEEE Transactions on Circuits and Systems-I:, vol. 69, no. 5, pp. 2035-2048, Feb 2022.

[3] Suchang Kim et al, "Real-time SSDLite Object Detection on FPGA", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 29, no. 6, pp. 1192-1205, June 2021.

<Professor Hyeon-min Bae's Lab.>

NAIS Nanoscale Advanced Integrated Systems LAB

■ **Contact information**

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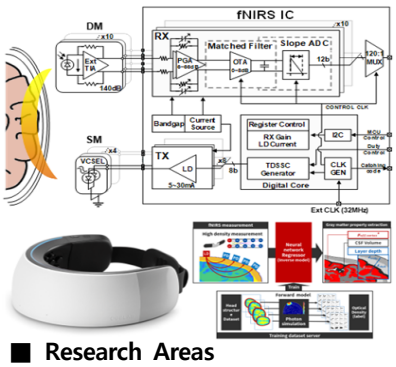
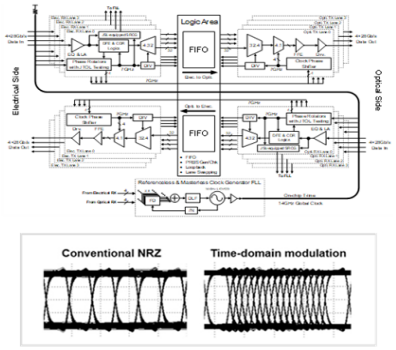
■ **Current state of the Lab. (in 2023 Fall Semester)**

Postdoctoral Fellows : 1 PhD Students: 5 Master's Student: 10

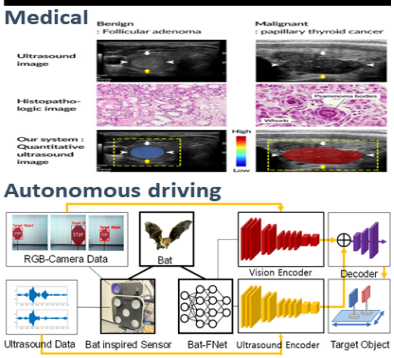
fNIRS System



High-Speed Circuit



Ultrasound System



■ **Research Areas**

At NAIS lab, we engage in a wide range of research regarding various application fields based on high-speed communication integration circuit technology. As the research topics take system-wide approach, students will be able to experience and accumulate broad spectrum of knowledge during the process of completing the research. The objective of all research performed at NAIS lab is to implement and commercialize innovative systems through disruptive technology. NAIS lab encourages students to experience venture ecosystem by getting involved in establishing ventures based on the research performed during the graduate school years. OBELAB and Poin2Tech are start-ups that were established, based on the research conducted during the graduate school years at NAIS lab. Alumnis are strongly involved in those companies.

■ **Recommended courses & Career after graduation**

One of the most important virtue at NAIS lab is 'craftsmanship'. For this, NAIS lab focuses on research and development involving communication circuits, and it is recommended that students take courses in circuit, digital, and communication-related subjects. Graduates of NAIS lab pursue careers both in industry and academia. They seek to enhance the degree of completion of their own research carried out at NAIS lab.

■ **Introduction to other activities besides research**

We like to explore famous restaurants around Daejeon. Lab members are also active in physical activies.

■ **Introduction to the Lab.**

NAIS lab was established in 2009. It is constantly challenging and pursuing progress in many areas of research. The doctorate and the masters degree students are working in a friendly atmosphere. Students enjoy athletic activities and other hobbies. The lively atmosphere of the lab makes it possible for the students to devote themselves to research and to enjoy school life.

■ **Recent research achievements ('21~'23)**

[1] Woohyun Kwon, Hyosup Won, Taeho Kim, Ha-Il Song, Hanho Choi, Sejun Jeon, Soon-Won Kwon, Bongjin Kim, Huxian Jin, Jun-Gi Jo, Tai-Young Kim, Jake Eu, Jinho Park, Hyeon-Min Bae, "A 25.78125Gbps Bi-directional Transceiver with Frame-Pulsewidth Modulation(FPWM) for Extended Reach Optical Linkds in 28nm CMOS", 2022 IEE Symposium on VLSI Tchnology and Circuits, June 2022.

[2] Seok-Hwan Oh, Myeong-Gee Kim, Youngmin Kim, Guil Jung, Hyuksool Kwon, Hyeon-Min Bae, "Sensor geometry generalization to untrained conditions in quantitative ultrasound imaging", International Conference on Medical Image Computing & Computer Assisted Intervention (MICCAI), Sept.2022

[3] Myeong-Gee Kim, Seok-Hwan Oh, Youngmin Kim, Hyuksool Kwon, Hyeon-Min Bae, "Learning-based attenuation quantification in abdominal ultrasound", International Conference on Medical Image Computing & Computer Assisted Intervention (MICCAI), Sept.2021. - (early accept, top 13%)

<Professor Youngsoo Shin's Lab.>

DT LAB

Semiconductor Design Technology

■ Contact information

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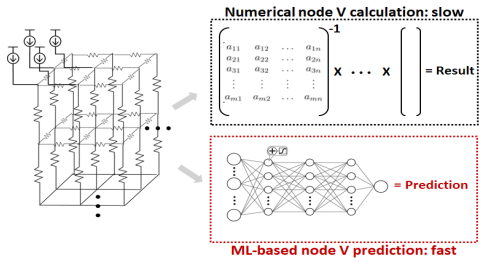
Website	http://dtlab.kaist.ac.kr	

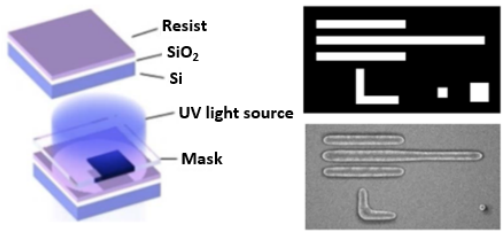
■ Current state of the Lab. (in 2022 Fall Semester)

Postdoctoral Fellows : 1 PhD Students: 6 Master's Student: 7

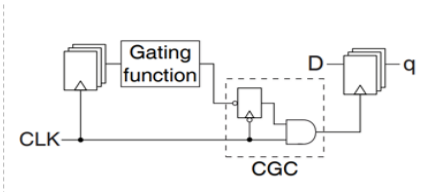
■ Research Areas



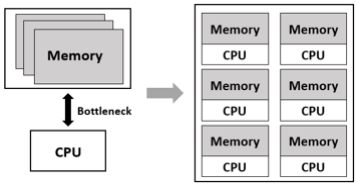
• **AI-EDA** Address challenges in electronic design automation (EDA) by using machine learning



• **Computational Lithography** Correct and verify mask to prevent distorted patterning by diffraction on wafer



• **Low Power Design** Reduce power consumption by supplying clock power only when clock is needed



• **Processing In Memory** Accelerate CPU operation without bottleneck between memory and CPU

■ Recommended courses

- Digital System (EE303) for undergraduate students
- CAD for VLSI (EE574) and Digital Integrated Circuit (EE678) for graduate students

■ Career after graduation

Most alumni entered leading semiconductor (**IBM, NVIDIA, Samsung Electronics, SK Hynix, and LG Electronics**) and EDA (**Synopsys, Cadence**) companies.

■ Introduction to other activities besides research

- Internship opportunities in **IBM, Synopsys, Siemens, Cadence (USA), and IMEC (Belgium)**
  - Ph.D. students had a chance to work abroad for the last few years
- Research sharing with Samsung S.LSI
- Workshop once a year (held in Jeju for this summer)
- Monthly social gatherings (coffee time, sports activities)

■ Introduction to the Lab

We all pursue excellent achievement with mutual encouragement. Our lab is the **top laboratory in the EDA research field** in Korea. Professors and students have extensive EDA-related knowledge. Also, **Mentoring system** is well established, so you can receive a lot of help in selecting research topics. Through our **collaborated projects with leading semiconductor companies**, we can research current hot issues of industry. Prof. Shin always welcomes personal meeting for detailed discussion on research topic, and he enthusiastically supports and motivates students.

■ Recent research achievements (2018-2023)

- Ph.D. Outstanding Dissertation Award in 2023, 2016, 2012
- Best paper award (including nominate): TSM'22, TSM'21, ASP-DAC'20, GLSVLSI'20
- Prof. Shin has been elected as IEEE Fellow and KAIST ICT Endowed Chair

⟨Professor Hoi-Jun Yoo⟩

Semiconductor System Laboratory

■ Contact information		
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Lab.	**sslmaster@kaist.ac.kr**	**Tel: 042-350-8068**
Website	**https://ssl.kaist.ac.kr**	

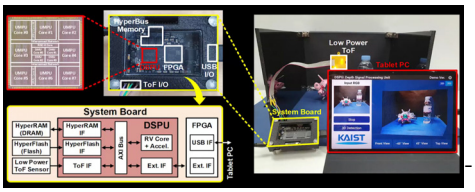
■ **Current state of the Lab. (in 2023 Fall Semester)**

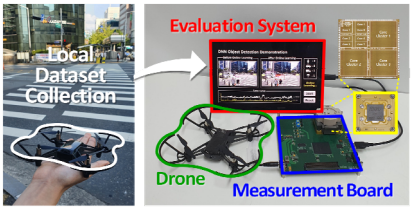
Postdoctoral Fellows : 0 PhD Students: 11 Master's Student: 10

■ **Research Areas**

Humanistic Intelligence System

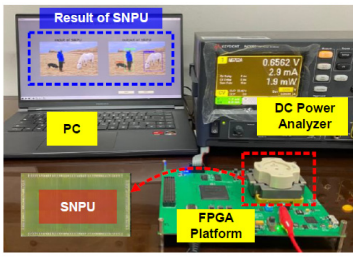
- Energy-Efficient Mobile DRL Training Processor
- World-First Floating-point Computing-in-Memory Architecture
- Multi-DNN Training Processor for Generative Adversarial Networks
- 3D Point Cloud-based Neural Network Processor
- CNN Super Resolution Processor for Full HD 60fps Video
- Mobile Neural 3D Rendering Processor
- eDRAM-based In-Memory-Computing Chip





Neuromorphic

- Always-on Face Recognition Spike Domain CNN Processor
- Neuromorphic Computing-in-Memory Processor
- Energy-efficient Analog-Digital Hybrid Computing Architecture
- Biological Neural Network System
- Complementary CNN/SNN Processor



■ **Recommended courses**

Circuit related courses (analog & digital), computer architecture, and digital systems will be helpful, but you can learn everything you need through OJT.

■ **Career after graduation**

Companies & research institutes all over the world (Apple, IBM, IMEC, Samsung, LG, etc.) or Universities (KAIST, UNIST, etc.)

■ **Introduction to other activities besides research**

In SSL, you will get a chance to explore international companies and research facilities like Samsung, IMEC, IME, Apple every year. Moreover, a joint workshop with Chinese (Tsinghua Univ.) and Japanese (Tokyo Univ.) universities is held every year. There are also lab workshops and parties with lab members.

■ **Introduction to the Lab**

Privilege of SSL Members

- Pride from world leading researches
- Business trip abroad average of 2 times per year
- Accepted to various international conferences/journals
- Project leading skills and presentation skills
- Semiconductor Chips with your name inscribed on

SSL Wants

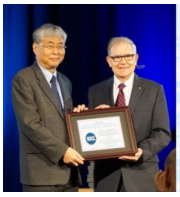
- Who has passion to be the best
- Who wants to become a world leading engineer

Statue of SSL

- You can directly feel it at international conferences

■ **Recent research achievements (2020-2023)**

- Top class international conferences: **6** ISSCC / **12** S. VLSI / **9** HotChips papers presented
- Major international papers: **46** journal / **62** conference papers accepted
- Awards: 2022 AICAS best paper/demo award, 2022 CICC outstanding paper award, 2020 ISSCC Demo Award, 2020 Humantech Gold Prize, etc.



<2022 AICAS Demo Award> **<2020 ISSCC Demo Award>** **<2020 Humantech Gold Prize>**

<Professor Wanyeong Jung's Lab.>

Smart Energy-Efficient Design Laboratory

■ Contact information

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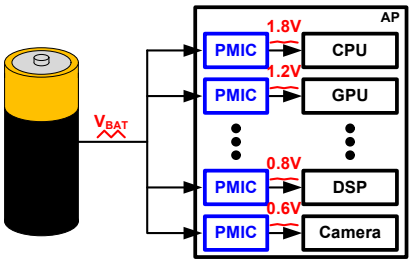
■ Current state of the Lab. (in 2023 Fall Semester)

Postdoctoral Fellows : 0 PhD Students: 10 Master's Student: 10 Undergraduate Student: 4

■ Research Areas

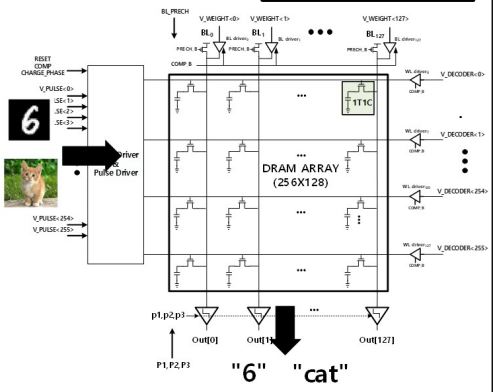
▶ Autonomous Power Management for Self-Powered Devices

Improving efficiency in energy harvesting and power management is essential to extend overall system operating time. The group has developed efficient switched-capacitor (SC) DC-DC converters for energy harvesting and power management. The group is also exploring inductive/hybrid DC-DC converters, multi-phase/multi-output converters, linear regulators, and their applications including fine-grained DVFS and design co-optimization with load circuits.



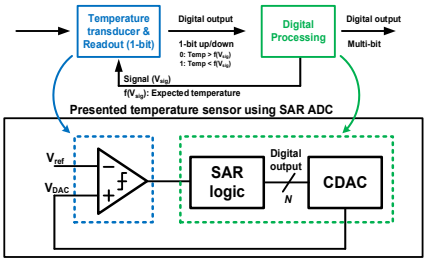
▶ Machine Learning on Edge Devices

Machine learning allows us to make a unified data processing accelerator that can be widely used in many applications and devices regardless of data type and purpose. The needs for machine learning are growing fast in many types of mobile devices and systems, but it is difficult to find an architecture with high efficiency and flexibility. The PI has developed a general inference accelerator for various types of CNN networks, and the group is now extending the research area to digital building blocks, computer architecture, near/in-memory computing with analog computation, and algorithm. The group is also trying to apply machine learning to circuit design process itself, to automate some time-consuming design steps.



▶ Energy-Efficient Sensors in Advanced Technologies

Sensor interfaces are difficult to scale down because of noise, process variations, and the reduction of output swing and intrinsic gain in advanced processes. The PI applied principles for digital circuits to analog designs so that they fully benefit from process scaling and are easily combined with other digital-oriented techniques. While trying to extend the application of this new approach among others, the group has developed many analog circuits including ADCs and sensor inferfaces, aiming for simpler and more robust design with efficiency.



■ Recommended courses & Career after graduation

Courses for analog and digital integrated circuits are strongly recommended. Basic English and programming skills are necessary. The career after graduation includes academia or industries related to circuit design.

■ Introduction to other activities besides research

The lab holds group dinners and annual workshop. The lab supports attendance at top international conferences in the field of integrated circuits such as ISSCC and VLSI-C, and other student-driven events and activities.

■ Introduction to the Lab.

The lab was established in August 2019. The lab is looking for graduate students and undergraduate students who are interested in IoT/low-power circuits and systems. The lab has friendly atmosphere and various research field, and try to research more creatively.

■ Recent research achievements ('21~'23)

[1] "A 74.0 dB-SNDR 175.4 dB-FoM Pipelined-SAR ADC Using a Cyclically Charged Floating Inverter Amplifier," *IEEE A-SSCC,* 2023
[2] "ConverGenT: Automated Topology Generation and Analysis of Hybrid DC-DC Converters," *IEEE TPEL*, June 2023
[3] "A Wide Range, Energy-Efficient Temperature Sensor Based on Direct Temperature–Voltage Comparison," *IEEE SSC-L*, April 2023

<Professor Minkyu Je's Lab.>

IMPACT Lab
Integrated Microsystems Powered with Advanced Circuit Technology

■ **Contact information**

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Lab. : ygc980215@kaist.ac.kr TEL : 7637

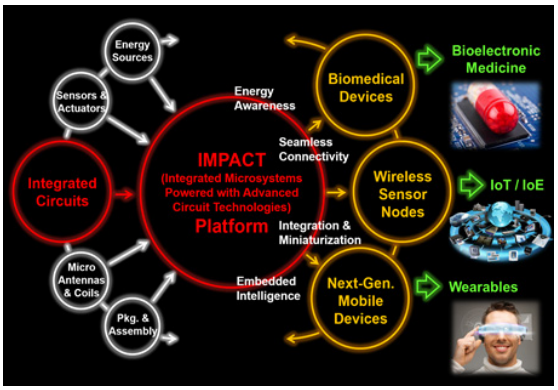
Website : impact.kaist.ac.kr

■ **Current state of the Lab. (in 2023 Fall Semester)**

Postdoctoral Fellows : 0 PhD Students: 26 Master's Student: 12

■ Research Areas

The core technology of the research is analog, mixed-signal, and RF integrated circuit design techniques, especially focusing on intelligent sensor interface circuits and ultra low power wireless communication circuits.



▷ **Intelligent sensor interface**

The sensor interface circuit that works with the sensor is an essential component to acquire the information of the real physical world. It has to provide sufficient performance while consuming low power. In particular, we aim to develop an intelligent interface circuit that can compensate the deficiencies of the sensor and extract meaningful information even under imperfect conditions.

▷ **Ultra-low-power wireless communication**

Particularly, we are interested in the technology that realizes the short distance communication in the vicinity of the human body with high energy efficiency as well as the various circuit techniques for duty-cycling the wireless communication circuits which consume the most power in the wireless sensor microsystems as much as possible.

▷ **Microsystem convergence for emerging applications**

Based on this low-power integrated circuit technology, the extremely small and intelligent systems can be integrated for various applications expected to play an important role in the future. Especially, the miniaturized medical device that can be implanted inside a human body for therapeutics, brain research, and neuromodulation is the main application area. We are also interested in wearable devices which are expected to be the next generation mobile devices, and ultra low power wireless sensor nodes which are key to the implementation of the internet of things.

■ Recommended courses & Career after graduation

Courses on circuit and system design as well as wireless communication are recommended, which include circuit theory, electronic circuits, analog electronic circuits, digital electronic circuits, digital systems, digital signal processing, communication engineering, and radio engineering. After graduation, your career can be furthered at a variety of domestic and foreign companies, research institutes, or universities related to integrated circuit and microsystem design as well as research and development in the application areas of IoT, wearables, and medical devices.

■ Introduction to other activities besides research

The IMPACT lab. is fairly new in that we started in 2016 at KAIST. Therefore, the members can make an important contribution in forming the culture of the laboratory. The best possible support will be provided to create an environment in which the members can engage in research with pleasant passion, voluntary commitment, and open exchange, based on strong mutual trust. A variety of non-research activities are also being created in line with this.

■ Introduction to the Lab.

We are not just targeting to develop new circuit design techniques, but to create substantial achievement that can greatly affect our future lives, by working together with experts from diverse fields including sensor, energy, communication, packaging, as well as medical devices and IT applications through an international collaborative research network.

■ Recent research achievements (2022-2023)

[1] "A Process-Scalable Ultra-Low-Voltage Sleep Timer With a Time-Domain Amplifier and a Switch-Less Resistance Multiplier," IEEE Journal of Solid-State Circuits (JSSC), 2023.

[2] "A 2.5mW 12MHz-BW 69dB SNDR Passive Bandpass Delta-Sigma ADC with Highpass Noise-Shaping SAR Quantizers," IEEE Symposium on VLSI Circuits (SOVC), 2023.

[3] "A 187dB FoMS 46fJ/Conv. 2nd-order Highpass Delta-Sigma Capacitance-to Digital Converter," IEEE Symposium on VLSI Circuits (SOVC), 2023.

[4] "A High-Efficiency Single-Mode Dual-Path Buck-Boost Converter With Reduced Inductor Current," IEEE Journal of Solid-State Circuits (JSSC), 2023.

[5] "A 600mV$_{PP}$-Input-Range 94.5dB-SNDR NS-SAR-Nested DSM with 4th-Order Truncation-Error Shaping and Input-Impedance Boosting for Biosignal Acquisition," IEEE Symposium on VLSI Circuits (SOVC), 2022.

<Professor SeongHwan Cho's Lab.>

Cho's Circuits and Systems Laboratory (CCSLAB)

■ **Contact information**

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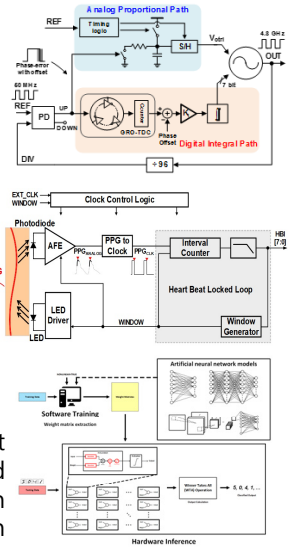
■ **Current state of the Lab. (in 2023 Fall Semester)**

Postdoctoral Fellows : 0 PhD Students: 11 Master's Student: 4

■ **Research Areas**

▷ High Speed Analog Circuits

The high speed analog circuits studied in our laboratory include clock generation, memory interface, and wireline transceiver. Representively, PLL is an essential analog and mixed-mode circuit which synthesizes system clock to the desired frequency for communication system. Recently, we are focusing on V-band(40-75GHz) and W-band(75-110GHz) PLLs for RADAR applications.



▷ PVT-invariant Sensors

High performance PVT-invariant sensors are one of our current research interests. In most applications, PVT variation degrades the performance of sensors. To relieve the trade-off between calibration cost and performance, we are currently focusing on developing related techniques for biomedical, environmental and automotive sensors

▷ Machine Learning Processors

Machine learning based on neural network has garnered great interest over the past decade as it has the potential to revolutionize various technologies for commercial and industrial use. In particular, we are interested to implement machine learning processor in analog circuit domain which is effective to achieve low-power and high-speed operation than digital domain.

■ **Recommended courses & Career after graduation**

Students are encouraged to take Circuit Theory, Electronic Circuits, Communication System, Introduction to Physical Electronics and Digital Signal Processing. Alumni are working with international major companies and research institutes such as DGIST, ETH Zurich, KAIST (Faculty), NVidia, Qualcomm, Broadcom, A*STAR, Samsung Electronics, Fairchild, MIT, Stanford, Univ. of Michigan, U. C. San Diego, MIT Sloan (MBA), and T. U. Delft.

■ **Introduction to other activities besides research**

We take annual/seasonal events such as strawberry party (spring season), ski camp and workshop to foster friendship. Also, members can have flexible vacation plan during the year to refresh and reinforce their motivation. We offer various opportunities to participate in international conferences.

■ **Introduction to the Lab.**

Our group explores emerging technologies for high-performance communication and interference-tolerant sensors. Research focus is on the design of analog integrated circuits with multiple layers of system abstraction in mind, from algorithms and system architectures to circuit techniques and devices. Our main research area is wireline data interface, CMOS sensors, phase-locked loops (PLL), and low power circuit for machine learning. Recently we are also looking into power management circuit as well as reference generator.

■ **Recent research achievements ('21~'23)**

[1] J.-O. Seo, M. Seok, S.H. Cho, "ARCHON: A 332.7TOPS/W 5b Variation-Tolerant Analog CNN Processor Featuring Analog Neuronal Computation Unit and Analog Memory" IEEE International Solid-State Circuits Conference (ISSCC), 2022.

[2] Y. Jung, S. Lee, H. Kim, S.H. Cho, "A Supply-Noise-Induced Jitter-Cancelling Clock Distribution Network for LPDDR5 Mobile DRAM featuring a 2nd-order Adaptive Filter" IEEE International Solid-State Circuits Conference (ISSCC), 2022.

[3] N. Koo, H. Kim, and S.H. Cho. "A 43.3uW Biopotential Amplifier With Tolerance to Common-Mode Interference of 18Vpp and T-CMRR of 105 dB in 180-nm CMOS." IEEE Journal of Solid-State Circuits, 2022.

[4] S. Park, J-H. Seol, L. Xu, S.H. Cho, D. Sylvester, and D. Blaauw, "A 43 nW, 32 kHz, A 43 nW, 32 kHz, ±4.2 ppm Piecewise Linear Temperature-Compensated Crystal Oscillator With ΔΣ-Modulated Load Capacitance", IEEE J. Solid-State Circuits, vol. 57, no. 4, 2022.